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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,612	09/16/2003	Steven Driediger	1400.1375170	3514

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,612	DRIEDIGER, STEVEN	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 are presented for examination.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Abstract

3. The abstract of the disclosure is objected to because it exceeds 150 words.

Applicant is reminded of the proper language and format for an abstract of the disclosure. **The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words.** It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "the disclosure defined by this invention," "the disclosure describes," etc. 2. The abstract of the disclosure is objected to because the abstract exceeds 150 words. Correction is required. See MPEP j 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims **1, 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37, 38** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claim 1 recites, **"the key** jointly define" (see line 4), which renders the claim indefinite. It is unknown if the applicant is referring to the said "a key based-protection".

b) Claims 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37 and 38 recite the phrase "adapted for" since languages that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims **1-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (6,597,595).

As per claims 1 and 12:

Ichiriu in figure 25 discloses a CAM device (700) includes an error CAM (715) to assert a match error signal (732) if a match index (174) matches any of a plurality of error addresses. In addition to the error CAM, the CAM device includes an address circuit (103), comparand register (115), and error detection circuit (711). Further, the address circuit, comparand register is coupled to one another and operates generally. Furthermore, an error detection circuit (711), for example, by the parity check circuit (201) and logic gate (222) described above in reference to FIG. 6 is coupled to receive the selected CAM word and output an error signal (712) to the error CAM (715). The error detection circuit asserts the error signal upon detecting an error in the selected CAM word and deasserts the error signal if no error is detected (see col. 24, lines 10-41). Ichiriu **does not explicitly** detailed the aspect of comparing predetermined protection word with the key-based protection word for indicating errors "as recited in claim 1". **However,** Ichiriu in FIG. 24, teach that a match error detector (705) is a

compare circuit that compare bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67) which the system of Ichiriu is basically employing the same method as the inventor's invention to detect errors. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to substitute the method of detecting errors and match error detector of Ichiriu with the claimed method for comparing protection word (CRC word) and error detection. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high reliable in operation.

As per claims 2 and 3:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Ichiriu disclosed that the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and in an alternative embodiments the comparand register may be omitted and the comparand value input directly to the CAM array from the comparand bus (see col. 3 lines 58-64).

As per claims 4 and 5:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Ichiriu disclosed in FIG. 6, the compare circuit (208) compares the output of the parity generator (206) with the corresponding stored parity bit. Compare circuit 208 is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic "1" only if the stored parity bit and the parity bit generated by the parity generator

do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuits 208 are logically ORed in gate (221) so that, if any one of the compare circuits 208 signals a mismatch (see col. 9, lines 33-43).

As per claims 6-11:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compare bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67).

As per claims 13-15:

Most of the limitations of these claims have been noted in the rejection of claim 12. In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67).

As per claim 16:

Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a CAM memory (102) coupled to error detector (107) wherein the CAM memory had and input and output.

As per claims 17-19:

Ichiriu teaches all the subject matter claimed in claim 16 including Ichiriu in figure 6 disclosed a parity generator for generating parity bits. In addition Ichiriu disclosed in FIG. 6, the compare circuit (208) compares the output of the parity generator (206) with

the corresponding stored parity bit. Compare circuit (208) is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic "1" only if the stored parity bit and the parity bit generated by the parity generator do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuits (208) are logically ORed in gate (221) so that, if any one of the compare circuits signals a mismatch (see col. 9, lines 33-43).

As per claims 20-22:

Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a comparand register (115) coupled to a CAM memory (101) and further the CAM memory coupled to an error detector (107).

As per claims 23-26:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67)

As per claims 27 and 28:

Ichiriu in figure 25 discloses a CAM device (700) includes an error CAM (715) to assert a match error signal (732) if a match index (174) matches any of a plurality of error addresses. In addition to the error CAM, the CAM device includes an address circuit (103), comparand register (115), and error detection circuit (711). Further, the address circuit, comparand register is coupled to one another and operates generally. Furthermore, an error detection circuit (711), for example, by the parity check circuit

(201) and logic gate (222) described above in reference to FIG. 6 is coupled to receive the selected CAM word and output an error signal (712) to the error CAM (715). The error detection circuit asserts the error signal upon detecting an error in the selected CAM word and deasserts the error signal if no error is detected (see col. 24, lines 10-41). Ichiriu **does not explicitly** detailed the aspect of comparing predetermined protection word with the key-based protection word for indicating errors "as recited in claim 1". **However,** Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67) which the system of Ichiriu is basically employing the same method as the inventor's invention to detect errors. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to substitute the method of detecting errors and match error detector of Ichiriu with the claimed method for comparing protection word (CRC word) and error detection. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high reliable in operation.

As per claims 29 and 30:

Most of the limitations of these claims have been noted in the rejection of claim 28. In addition Ichiriu disclosed that the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and in an alternative embodiments the comparand register

may be omitted and the comparand value input directly to the CAM array from the comparand bus (see col. 3, lines 58-64).

As per claims 31 and 32:

Most of the limitations of these claims have been noted in the rejection of claim 28. In addition Ichiriu disclosed in FIG. 6, the compare circuit (208) compares the output of the parity generator (206) with the corresponding stored parity bit. Compare circuit (208) is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic "1" only if the stored parity bit and the parity bit generated by the parity generator do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuits 208 are logically ORed in gate (221) so that, if any one of the compare circuits 208 signals a mismatch (see col. 9, lines 33-43).

As per claims 33-38:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67)

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 7,002,823 Ichiriu Michael E.

US PN: 6,978,301 Ichiriu Michael E.

US PN: 6,947,301 Regev et al.

US PN: 6,944,039 Nataraj et al

US PN: 6,914,795 Srinivasan et al

7. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

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